AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-5. (Canceled)

6. (Currently Amended) An active matrix display device ~~having~~ comprising an electro-optical modulating layer disposed between a pair of substrates, said active matrix display device comprising:

a plurality of column lines and a plurality of row lines supported by one of the substrates and defining a plurality of pixels in a matrix form;

a plurality of pixel electrodes formed in said plurality of pixels and supported by said one of said substrates;

a thin film transistor disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines;

a memory circuit disposed in each of said pixels and electrically connected to said thin film transistor, wherein said memory circuit stores an information output by said thin film transistor, wherein the memory circuit comprises a pair of inverters, each of the inverters comprising an n-channel thin film transistor and a p-channel thin film transistor, wherein an input of one of the pair of inverters is connected to the thin film transistor and an output of the other one of the pair of inverters, and wherein an output of the one of the pair of inverters is connected to an input of the other one of the pair of inverters and one of the plurality of pixel electrodes;

at least two voltage source lines electrically connected to said memory circuit; and

an opposite electrode on the other of said substrates,

wherein different voltages are applied to said pixel electrodes through said at least two voltage source lines based on the information stored by the corresponding memory circuit;

~~wherein said memory circuit comprises a pair of inverters connected to each other, each of said inverters comprising an N-channel TFT and a P-channel TFT; and~~

wherein an AC voltage having an amplitude equivalent to that of the voltages output of the memory circuit is supplied to the opposite electrode~~, and~~

~~wherein an output of the memory circuit is directly connected with a corresponding one of the plurality of pixel electrodes~~.

7. (Canceled)

8. (Previously Presented) The active matrix display device of claim 6 wherein the number of pixel electrodes equals the number of the digital memory circuits.

9. (Original) The active matrix display device of claim 6 wherein the active matrix display device includes a digital gradation display device.

10. (Original) The active matrix display device of claim 6 wherein the active matrix display device includes a time gradation display device.

11. (Original) The active matrix display device of claim 6 wherein the different voltages include a high voltage and a low voltage.

12. (Currently Amended) An active matrix display device ~~having~~ comprising an electro-optical modulating layer disposed between a pair of substrates, said active matrix display device comprising:

a plurality of column lines and a plurality of row lines supported by one of the substrates and defining a plurality of pixels in a matrix form;

a plurality of pixel electrodes formed in said plurality of pixels and supported by said one of said substrates;

a first thin film transistor disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines;

a memory circuit disposed in each of said pixels and electrically connected to said first thin film transistor, wherein said memory circuit stores an information output by said first thin film transistor;

at least two voltage source lines electrically connected to said memory circuit; and

an opposite electrode on the other of said substrates,

wherein different voltages are applied to said pixel electrode through said at least two voltage source lines based on the information stored by the corresponding memory circuit, and

wherein said memory circuit comprises at least second and third thin film transistors, one of source or drain of the second thin film transistor being connected with one of said voltage source lines, a gate electrode of the third thin film transistor, and one of source or drain of the first thin film transistor,

the other of source or drain of the second transistor being connected with the other of said voltage source lines and one of source or drain of the third thin film transistor, and

a gate electrode of the second thin film transistor being connected with the other of source or drain of the third thin film transistor, one of said voltage source lines, and said pixel electrode,

~~wherein said active matrix display includes a time gradation display device; and~~

wherein an AC voltage having an amplitude equivalent to that of the voltages output of the memory circuit is supplied to the opposite electrode~~, and~~

~~wherein an output of the memory circuit is directly connected with a corresponding one of the plurality of pixel electrodes~~.

13. (Previously Presented) The active matrix display device of claim 12 wherein a voltage supplied to the electro-optical modulating layer is substantially zero on time average.

14. (Previously Presented) The active matrix display device of claim 12 wherein the number of pixel electrodes equals the number of the memory circuits

15-16. (Canceled)

17. (Original) The active matrix display device of claim 12 wherein the different voltages include a high voltage and a low voltage.

18. (Currently Amended) An active matrix display device ~~having~~ comprising an electro-optical modulating layer disposed between a pair of substrates , said active matrix display device comprising:

a plurality of column lines and a plurality of row lines supported by one of the substrates and defining a plurality of pixels in a matrix form;

a plurality of pixel electrodes formed in said plurality of pixels and supported by said one of said substrates;

a first thin film transistor disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines;

a memory circuit disposed in each of said pixels and electrically connected to said first thin film transistor, wherein said memory circuit stores an information output by said first thin film transistor;

at least two voltage source lines electrically connected to said memory circuit; and

an opposite electrode on the other of said substrates,

wherein different voltages are applied to said pixel electrode through said at least two voltage source lines based on the information stored by the corresponding memory circuit,

wherein said memory circuit comprises at least two inverters, said inverters comprising at least two thin film transistors and being connected with said voltage source lines; and

wherein an input of one of the pair of inverters is connected to the thin film transistor and an output of the other one of the pair of inverters, and wherein an output of the one of the pair of inverters is connected to an input of the other one of the pair of inverters and one of the plurality of pixel electrodes;

wherein an AC voltage having an amplitude equivalent to that of the voltages output of the memory circuit is supplied to the opposite electrode~~, and~~

~~wherein an output of the memory circuit is directly connected with a corresponding one of the plurality of pixel electrodes~~.

19. (Previously Presented) The active matrix display device of claim 18 wherein the number of pixel electrodes equals the number of the memory circuits.

20. (Original) The active matrix display device of claim 18 wherein the active matrix display device includes a digital gradation display device.

21. (Original) The active matrix display device of claim 18 wherein the active matrix display device includes a time gradation display device.

22. (Original) The active matrix display device of claim 18 wherein the different voltages include a high voltage and a low voltage.

23. (Canceled)

24. (Currently Amended) An active matrix display device ~~having~~ comprising an electro-optical modulating layer disposed between a pair of substrates, said active matrix display device comprising:

a plurality of column lines and a plurality of row lines supported by one of the substrates and defining a plurality of pixels in a matrix form;

a plurality of pixel electrodes formed in said plurality of pixels and supported by said one of said substrates;

a first thin film transistor disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines;

a memory circuit disposed in each of said pixels and electrically connected to said first thin film transistor, wherein said memory circuit stores an information output by said first thin film transistor;

at least two voltage source lines electrically connected to said memory circuit; and

an opposite electrode on the other of said substrates,

wherein different voltages are applied to said pixel electrode through said at least two voltage source lines based on the information stored by the corresponding memory circuit,

wherein the memory circuit comprises at least second and third thin film transistors, one of source or drain of the second thin film transistor being connected with one of the two voltage source lines through a first resistor, a gate electrode of the third thin film transistor, and one of source or drain of the first thin film transistor,

the other of source or drain of the second transistor being connected with the other of the two voltage source lines and one of source or drain of the third thin film transistor, and

a gate electrode of the second thin film transistor being connected with the other of source or drain of the third thin film transistor, the one of the two voltage source lines through a second resistor, and the pixel electrode,

~~wherein said memory circuit comprises at least two thin film transistors, having a same conductivity type,~~

~~wherein said active matrix display device includes a time gradation display device, and~~

wherein an AC voltage having an amplitude equivalent to that of the voltages output of the memory circuit is supplied to the opposite electrode~~, and~~

~~wherein an output of the memory circuit is directly connected with a corresponding one of the plurality of pixel electrodes~~.

25. (Original) The active matrix display device of claim 24 wherein a voltage supplied to the electro-optical modulating layer is substantially zero on time average.

26. (Previously Presented) The active matrix display device of claim 24 wherein the number of pixel electrodes equals the number of the memory circuits.

27. (Original) The active matrix display device of claim 24 wherein the active matrix display device includes a digital gradation display device.

28. (Canceled)

29. (Original) The active matrix display device of claim 24 wherein the different voltages include a high voltage and a low voltage.

30-46. (Canceled)

47. (Previously Presented) The active matrix display device according to claim 6 wherein said electro-optical modulating layer comprises a liquid crystal.

48. (Previously Presented) The active matrix display device according to claim 12 wherein said electro-optical modulating layer comprises a liquid crystal.

49. (Previously Presented) The active matrix display device according to claim 18 wherein said electro-optical modulating layer comprises a liquid crystal.

50. (Previously Presented) The active matrix display device according to claim 24 wherein said electro-optical modulating layer comprises a liquid crystal.

51-54. (Canceled)

55. (Currently Amended) A method of operating an active matrix display device comprising the steps of:

storing a data in a memory circuit provided at one pixel;

supplying a voltage to a pixel electrode of said pixel in accordance with the data stored in said memory circuit; and

supplying an AC voltage to an opposite electrode opposed to the pixel electrode having an amplitude equivalent to that of the voltage output of the memory circuit,

wherein said memory circuit comprises at least first and second inverters, each inverter comprising [[one]] a p-channel [[type]] thin film transistor and [[one]] an n-channel [[type]] thin film transistor formed over a substrate, and

wherein an input of one of the pair of inverters is connected to an output of the other one of the pair of inverters, and wherein an output of the one of the pair of inverters is connected to an input of the other one of the pair of inverters and the pixel electrode.

~~wherein an output of the memory circuit is directly connected with the pixel electrode.~~

56. (Canceled)

57. (Currently Amended) A method of operating an active matrix display device comprising the steps of:

supplying a data through a switching thin film transistor provided at one pixel to a memory circuit;

storing said data in a memory circuit provided at said pixel; and

supplying one of two voltages from two voltage source lines to a pixel electrode of said pixel in accordance with the data stored in said memory circuit wherein said two voltage source lines are electrically connected to said memory circuit; and

supplying an AC voltage to an opposite electrode opposed to the pixel electrode having an amplitude equivalent to that of the voltage output of the memory circuit, and

~~wherein an output of the memory circuit is directly connected with the pixel electrode,~~

wherein said memory circuit comprises at least first and second inverters, each inverter comprising [[one]] a p-channel [[type]] thin film transistor and [[one]] an n-channel [[type]] thin film transistor formed over a substrate[[.]], and

wherein an input of one of the pair of inverters is connected to an output of the other one of the pair of inverters, and wherein an output of the one of the pair of inverters is connected to an input of the other one of the pair of inverters and one of the plurality of pixel electrodes.

58. (Canceled).

59. (Previously Presented) The method according to claim 57, wherein said display device is a liquid crystal device.

60. (New) The active matrix display device of claim 12 wherein the active matrix display includes a time gradation display device.

61. (New) The active matrix display device of claim 24 wherein the active matrix display includes a time gradation display device.